Hardware Accelerated SDR Platform for Adaptive Air Interfaces

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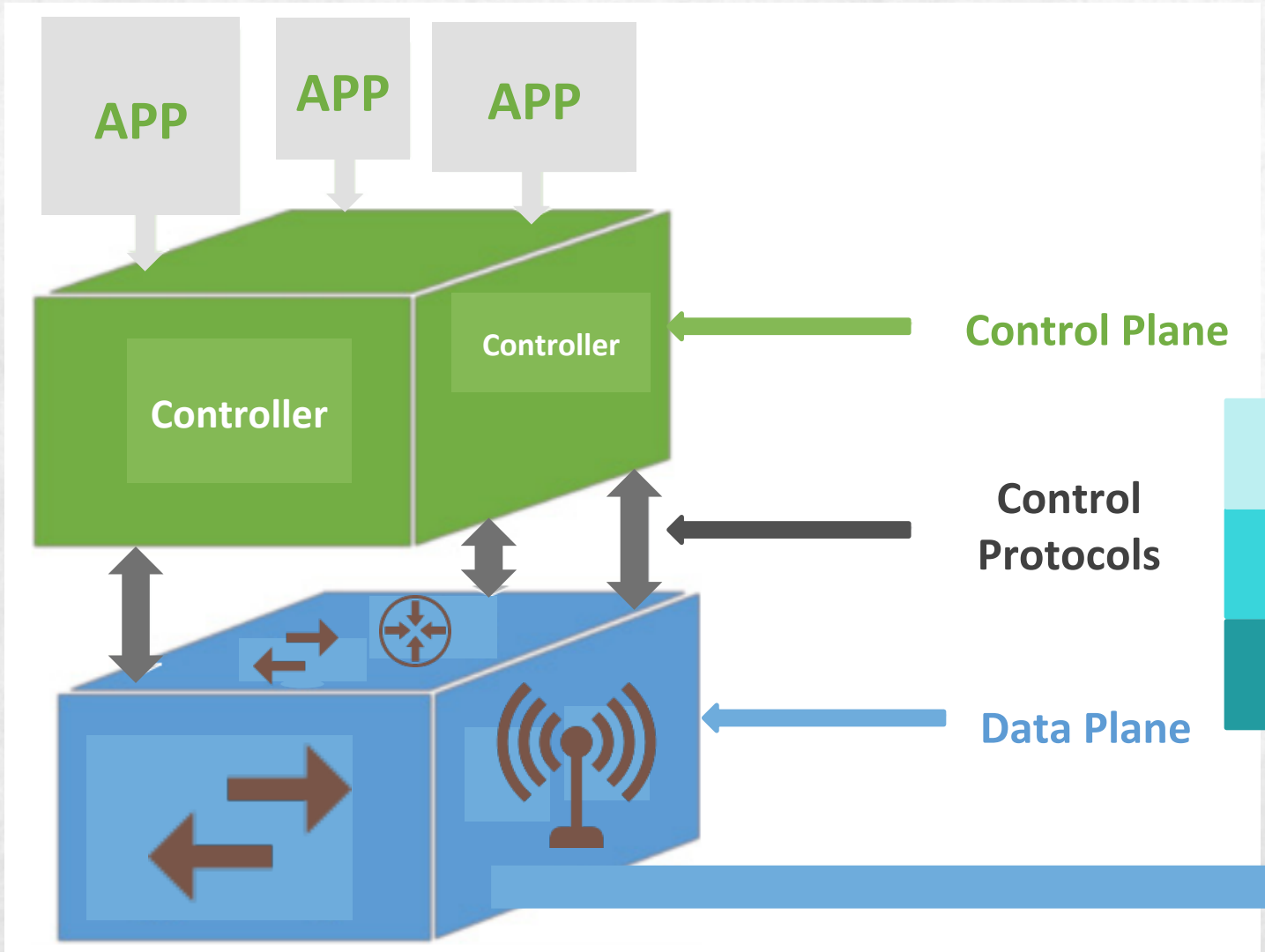
Overview

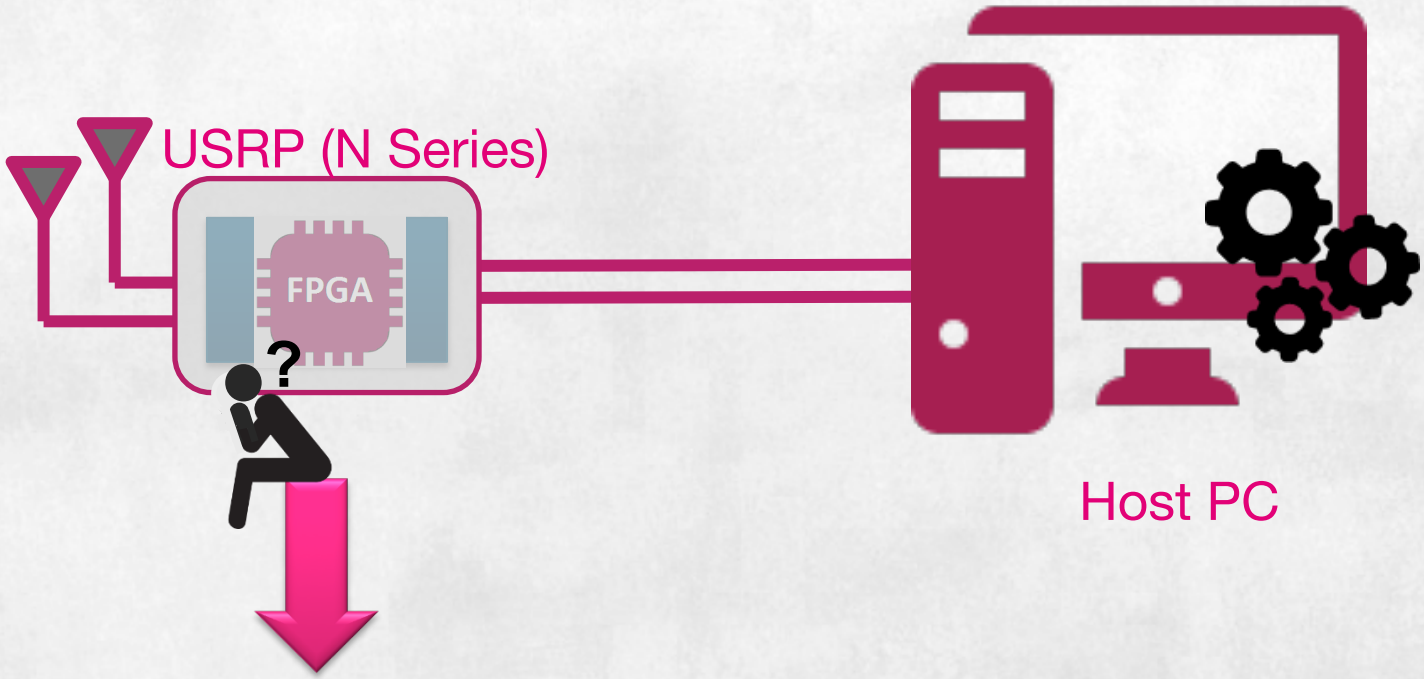
- Introduction
- Common SDR approach
- Propposed approach
- The future of computing
- Hardware accelerated SDR
- Example Use case

Introduction



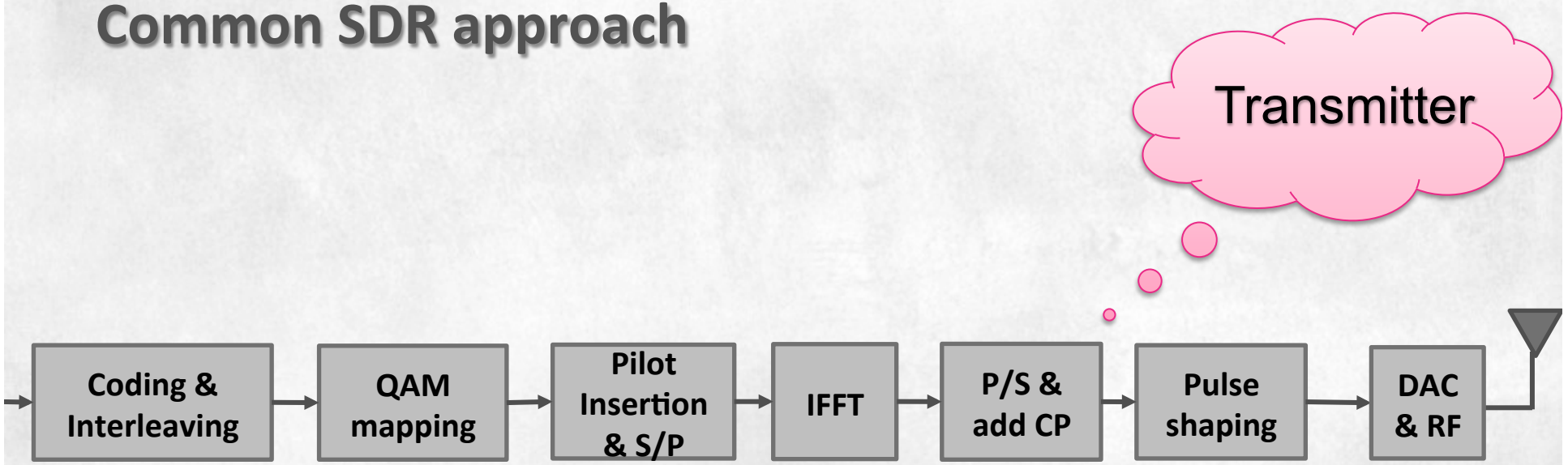
Common SDR approach

- Intensive signal processing is done in **host PC**
  - ***Real time processing is hard to achieve***
  - Significant power and space consumption (***no portability***)



- **FPGA** is ***seriously underutilized!***

Common SDR approach



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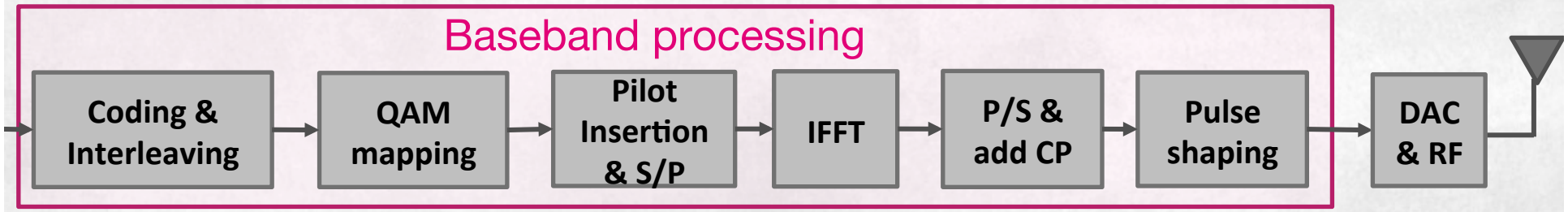
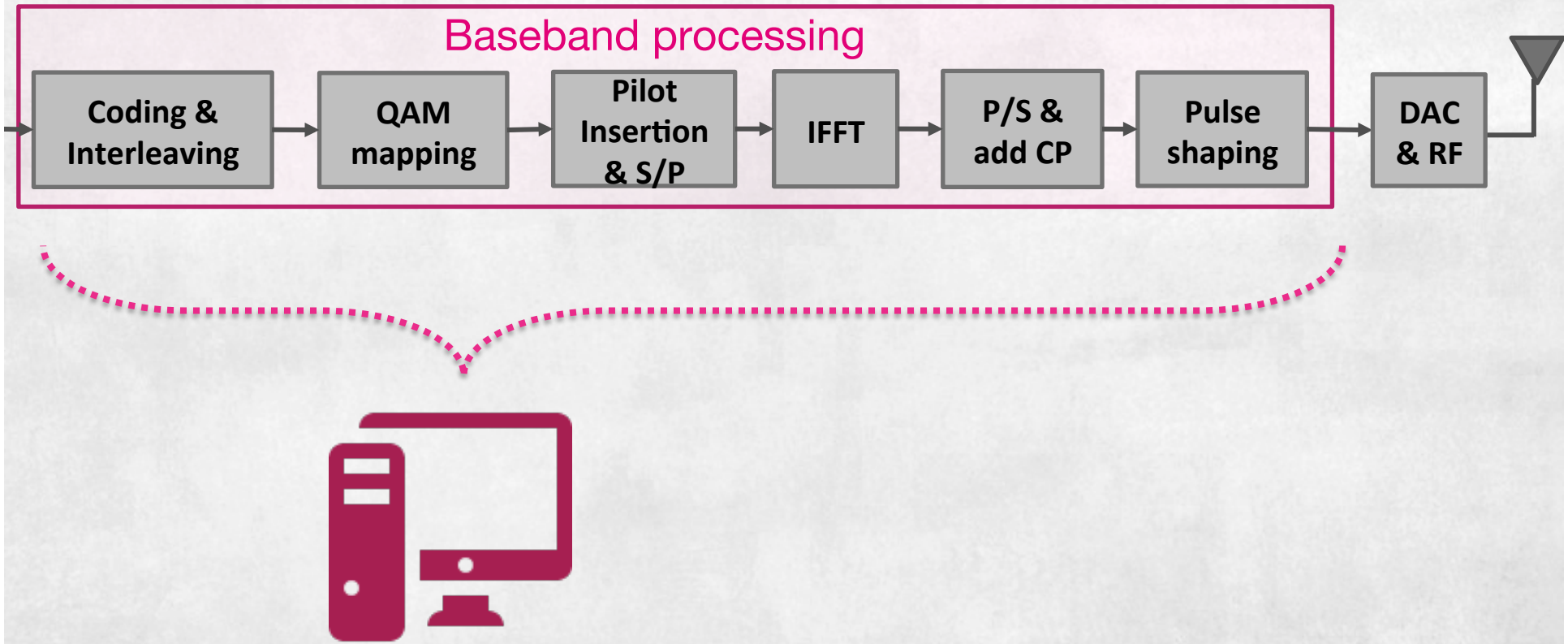
Common SDR approach



Common SDR approach



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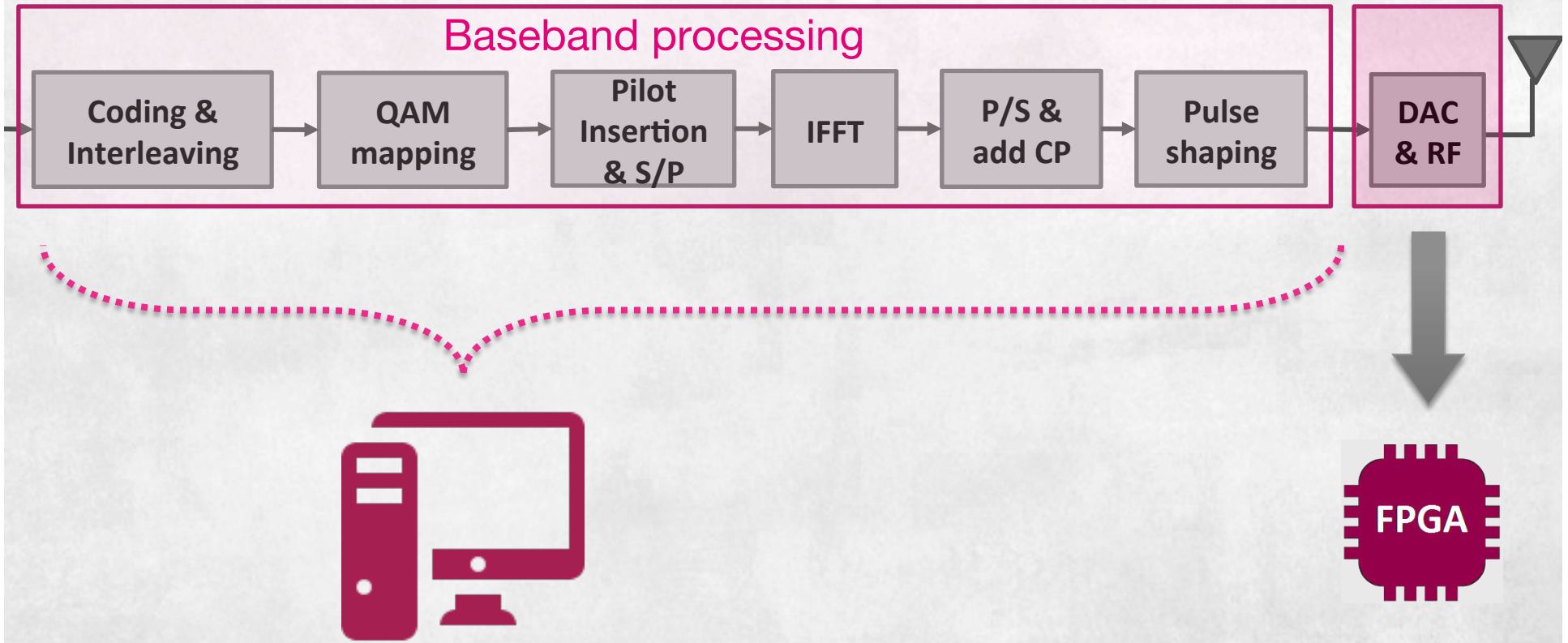
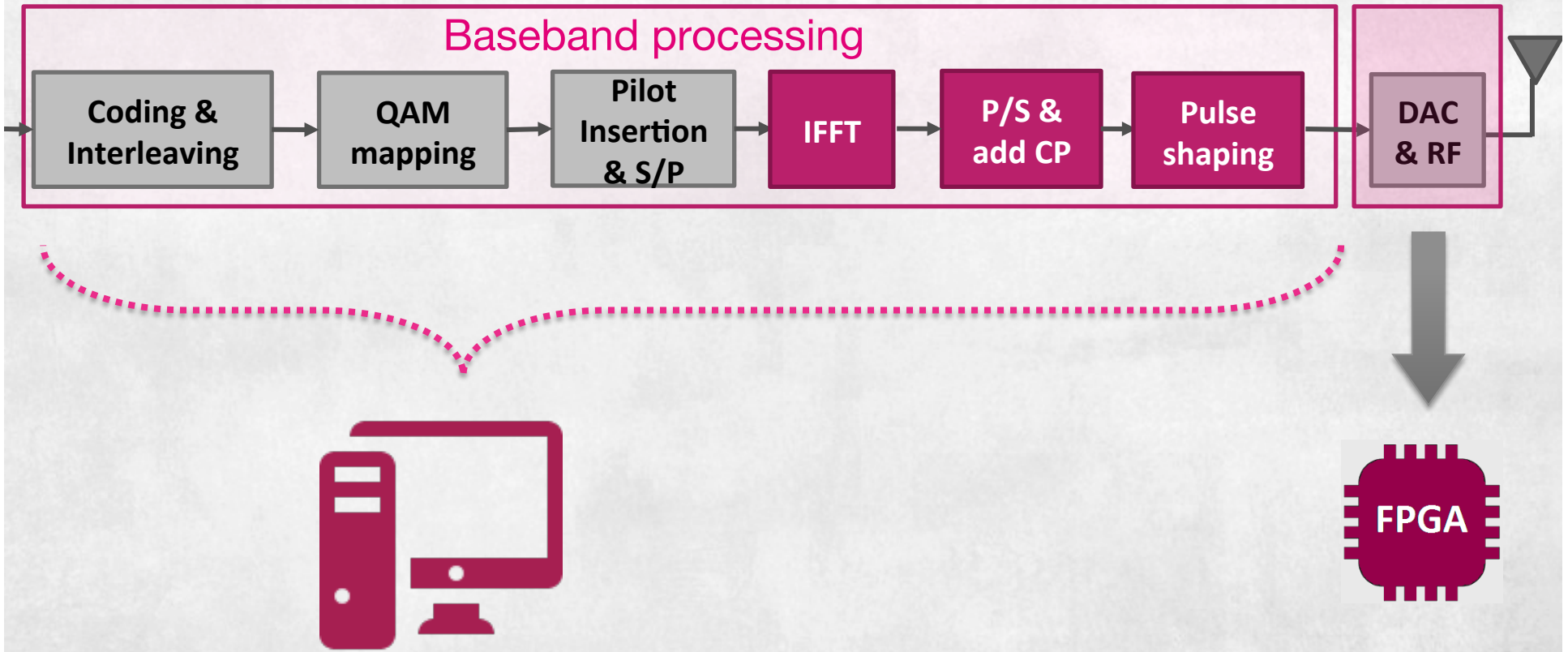
Common SDR approach



Common SDR approach



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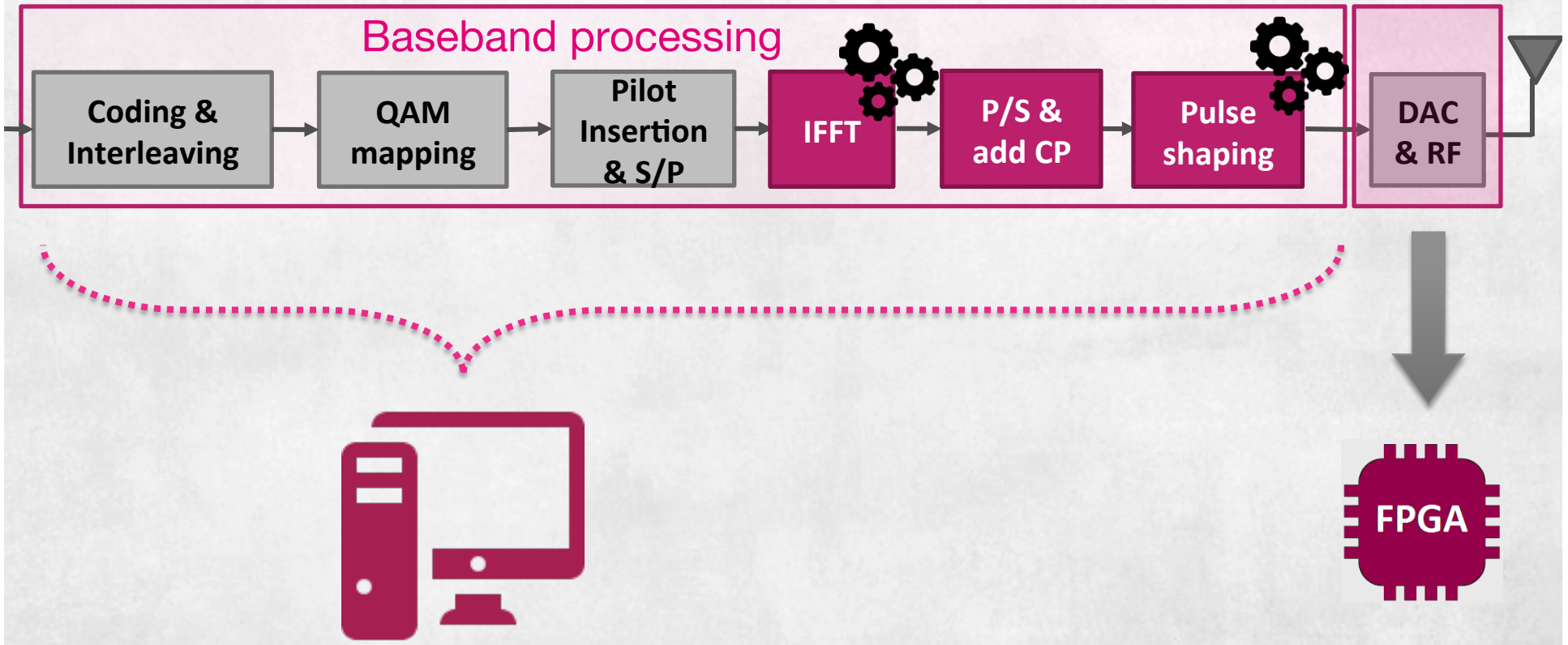
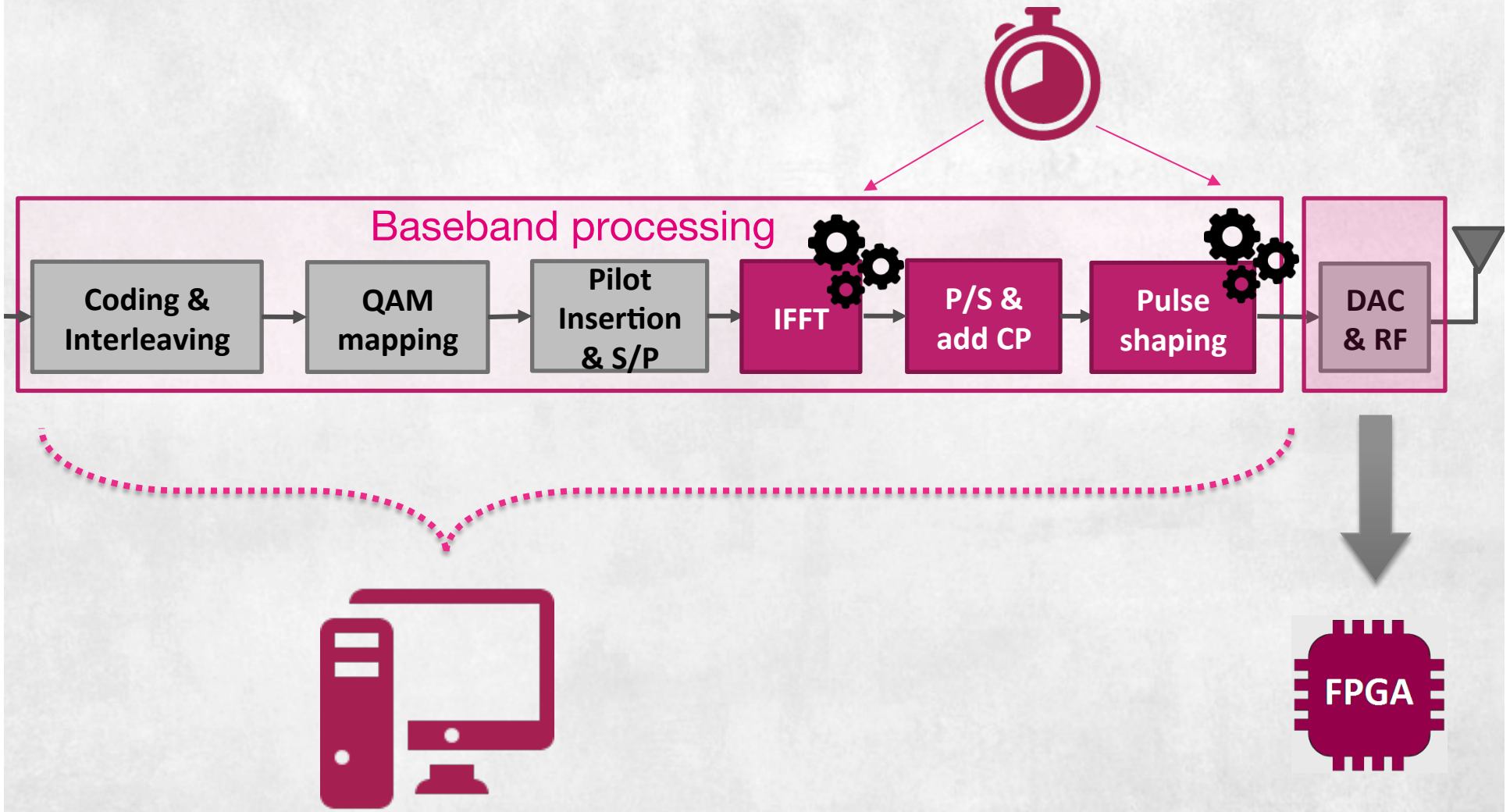
Common SDR approach



Common SDR approach



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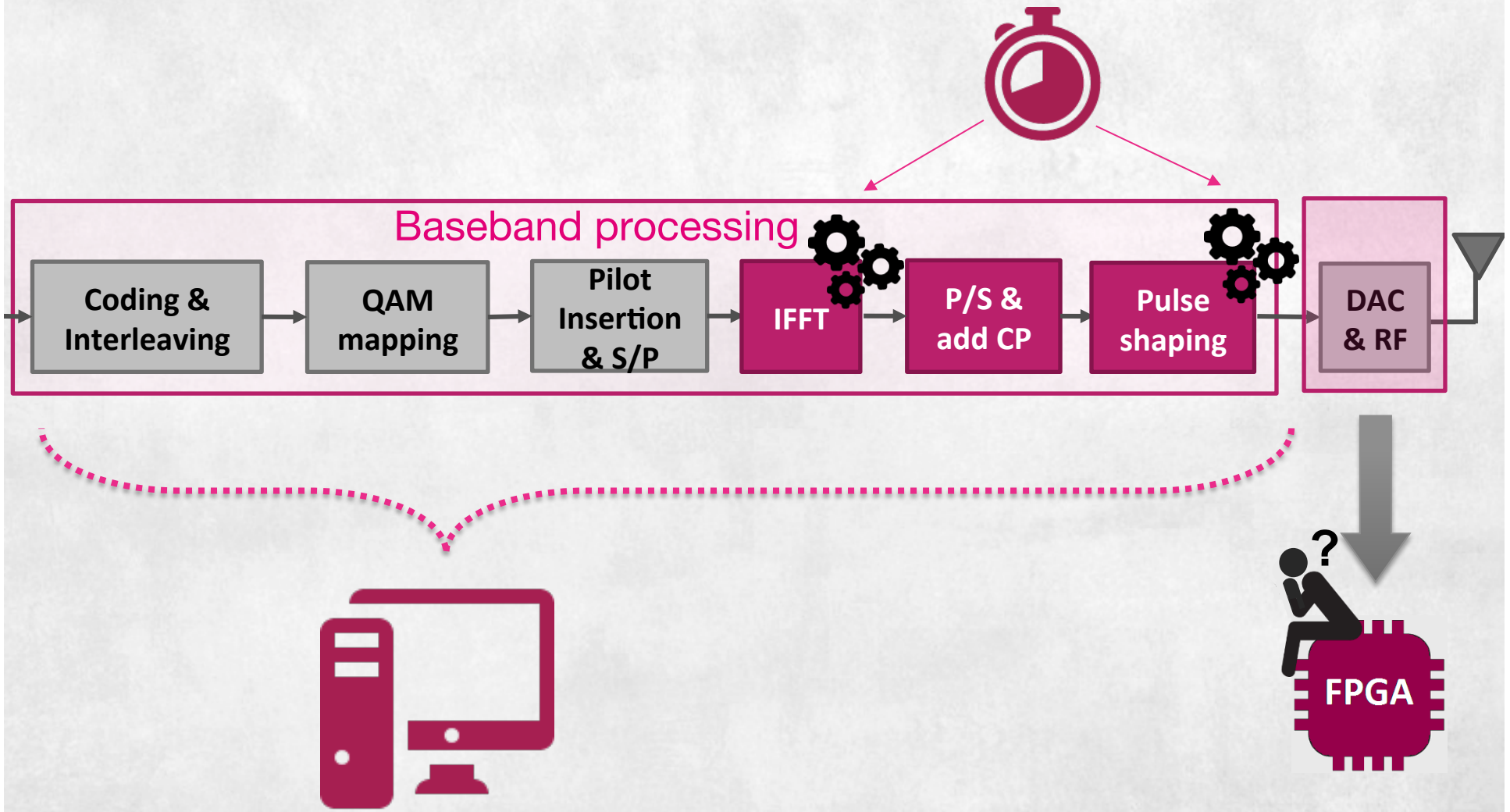
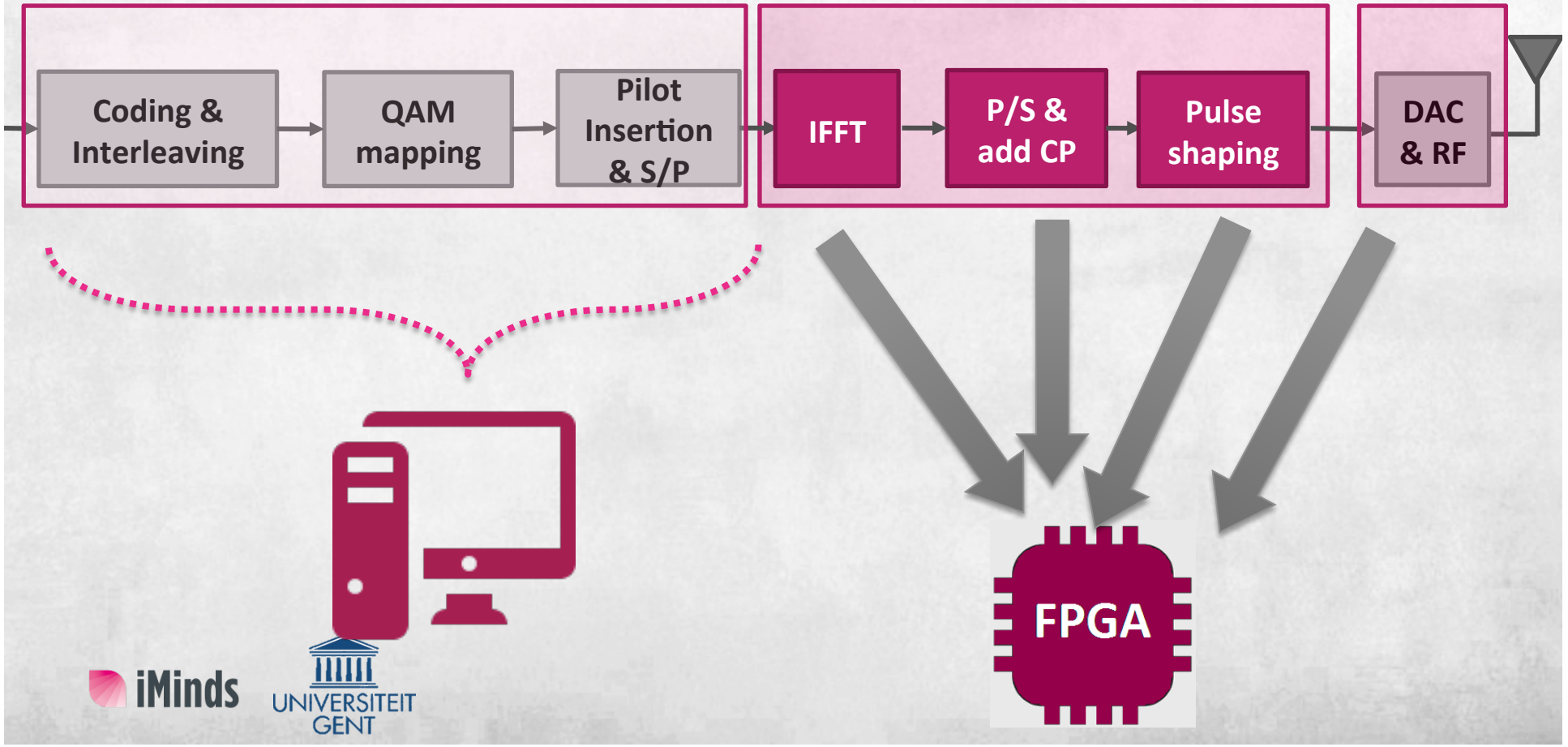
Common SDR approach



Proposed approach – Tx side



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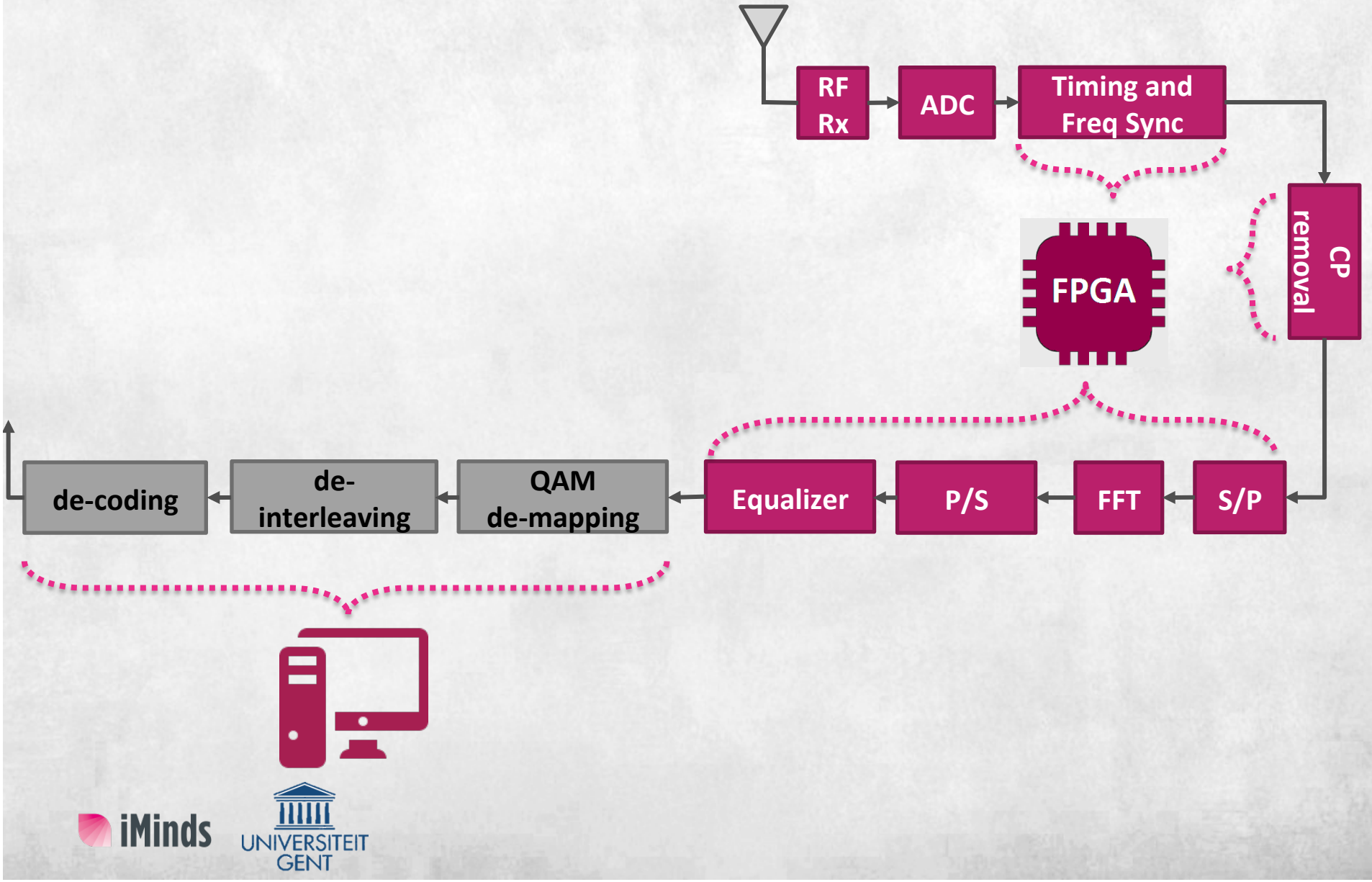
Proposed approach – Rx side



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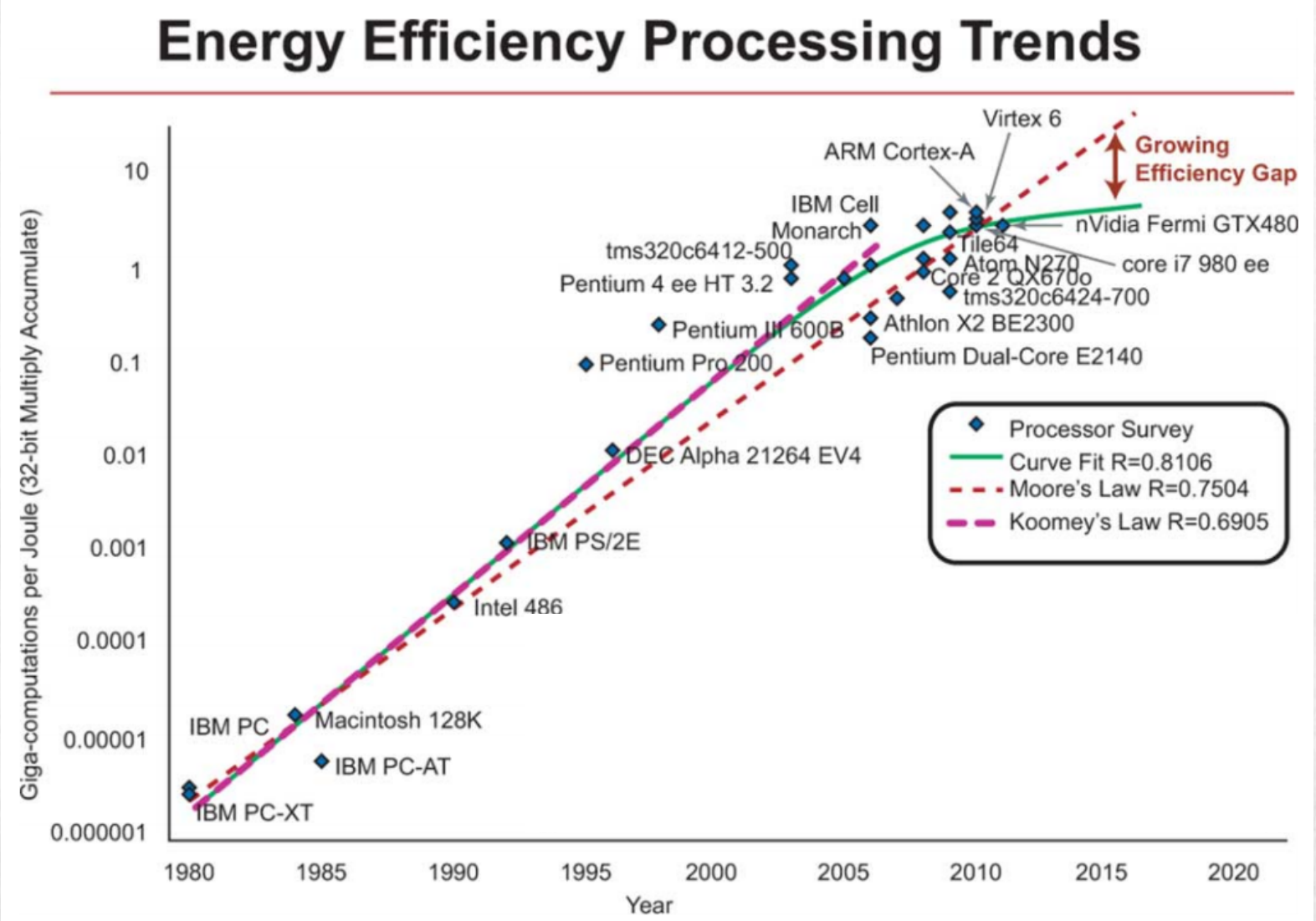
Current Pure Software Computing approach



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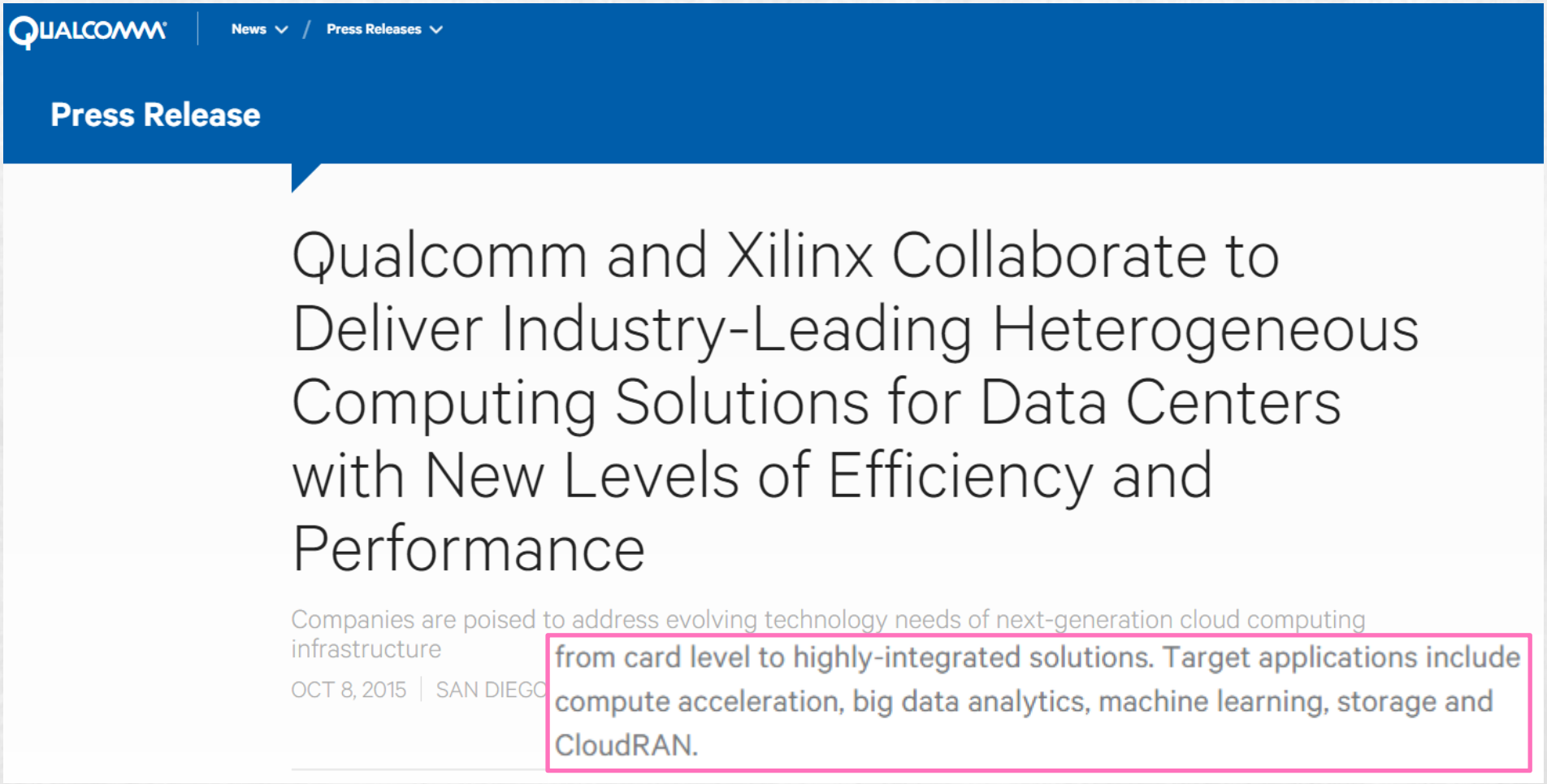
Sources: Marr et al., "Scaling Energy Per Operation via an Asynchronous Pipeline";
Koomey et al., "Implications of Historical Trends in the Electrical Efficiency of Computing"

Future computing – Hybrid Software & Hardware approach



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Source: Qualcomm website (01.17.2015)

Future computing – Hybrid Software & Hardware approach (1)

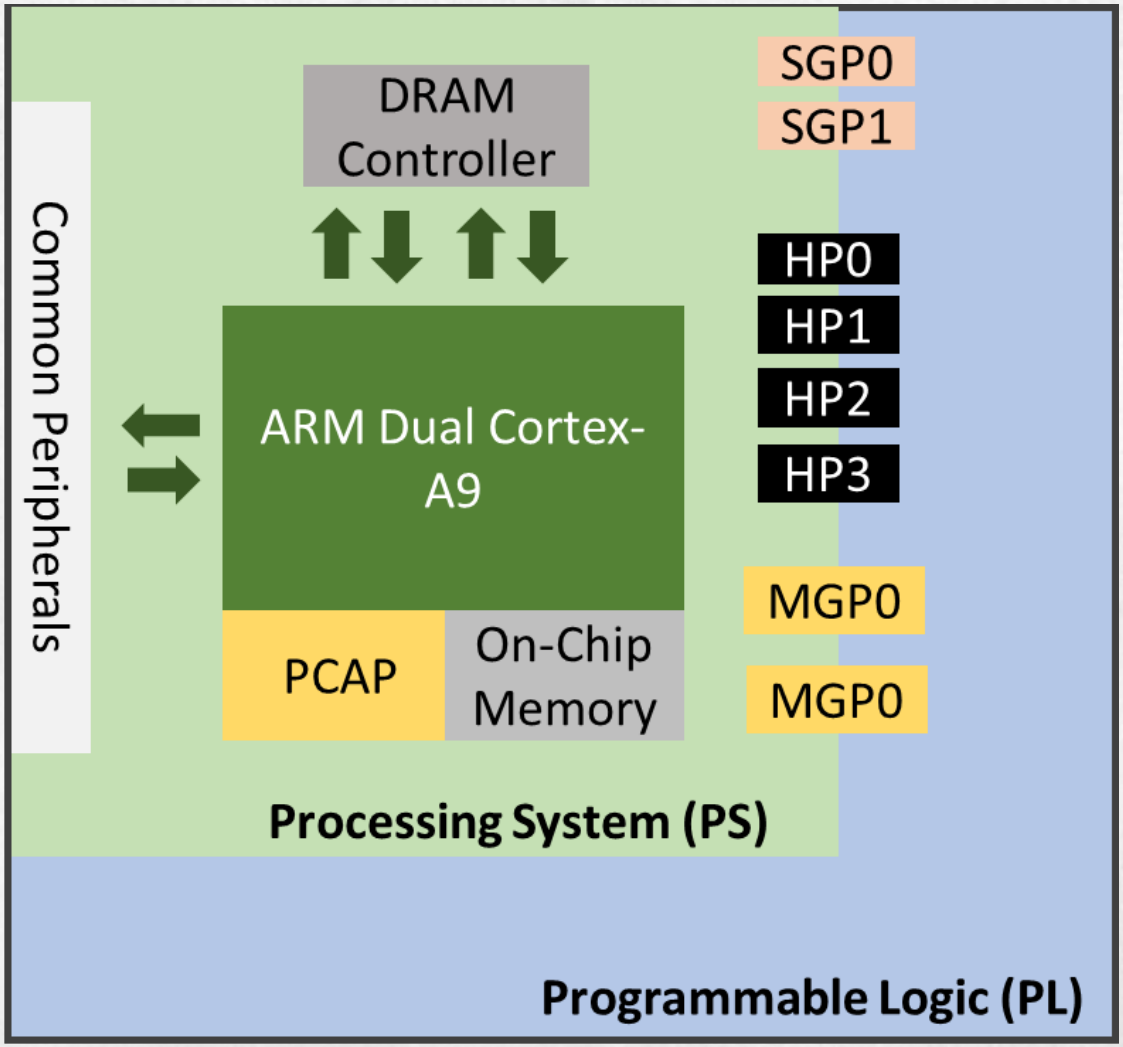
Welcome

Intel and Altera announced on June 1, 2015 that they entered into a definitive agreement under which Intel would acquire Altera for $54 per share in an all-cash transaction valued at approximately $16.7 billion. The transaction closed on December 28, 2015.

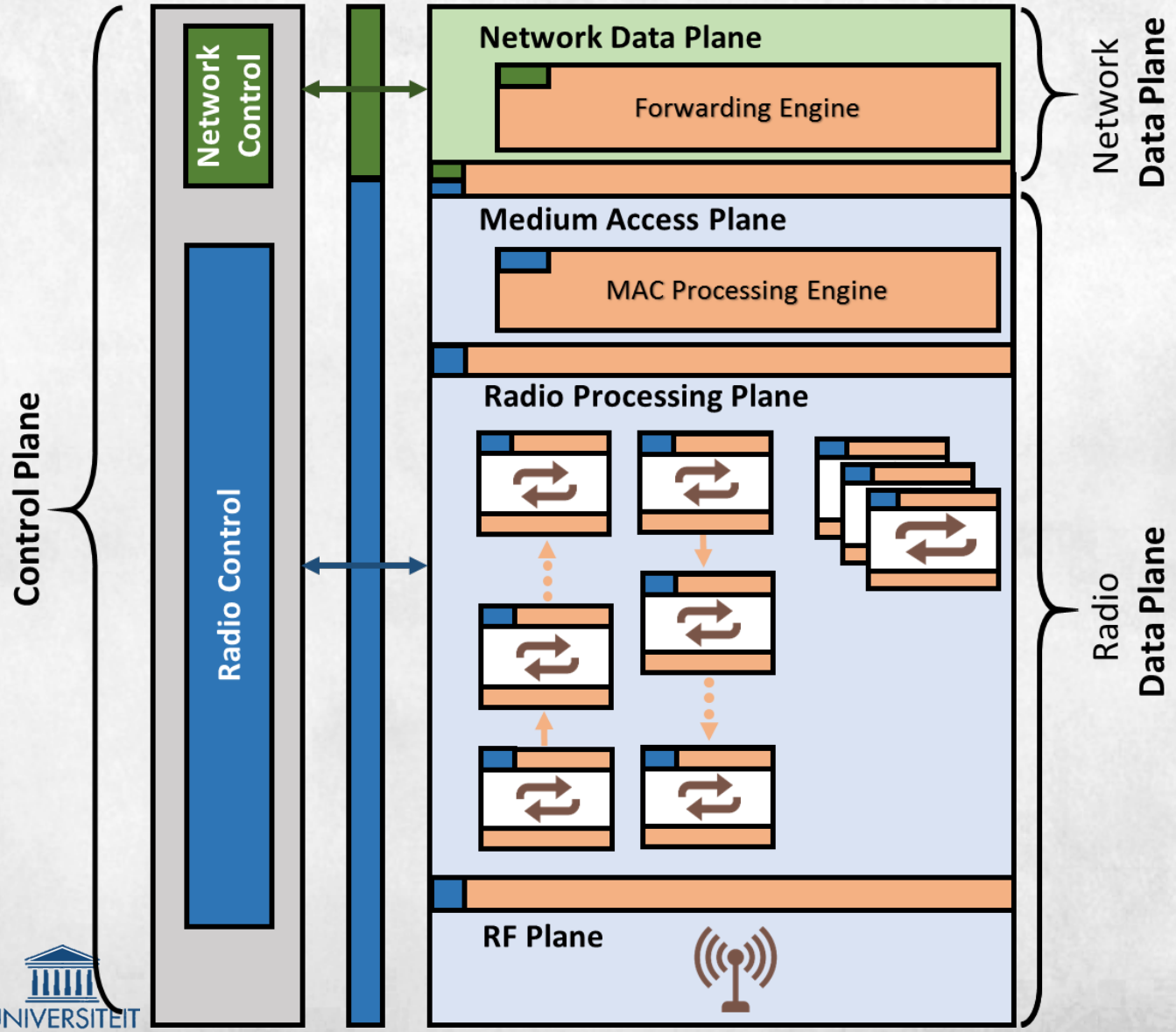
The acquisition will couple Intel's leading-edge products and manufacturing process with Altera's leading field-programmable gate array (FPGA) technology. The combination is expected to enable new classes of products that meet customer needs in the data center and Internet of Things (IoT) market

Source: Intel website (01.17.2015)

Hardware accelerated SDR platform on top of Hybrid FPGA



Hardware accelerated SDR platform on top of Hybrid FPGA (1)



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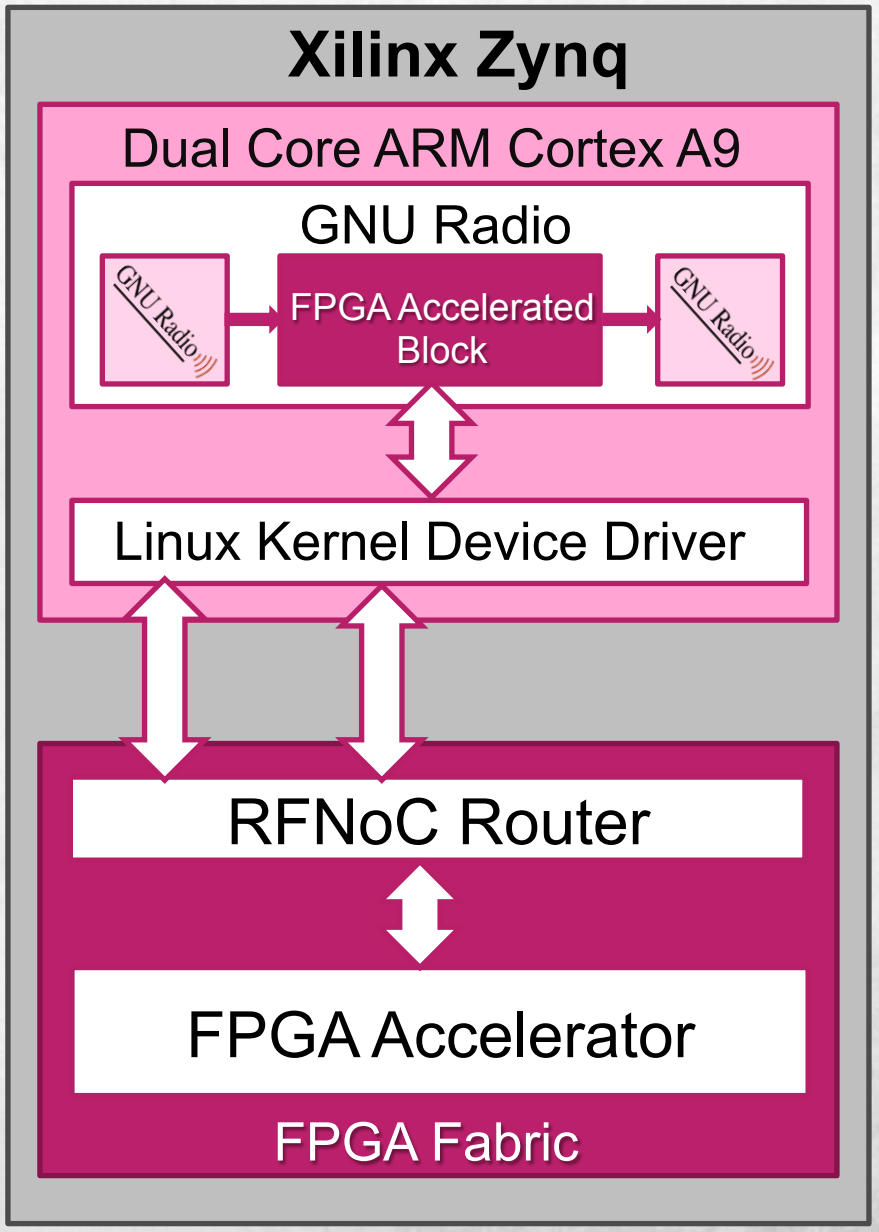
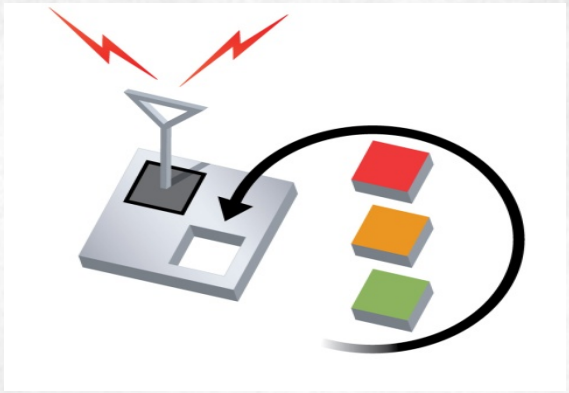
Hardware accelerated SDR platform on top of Hybrid FPGA (2)

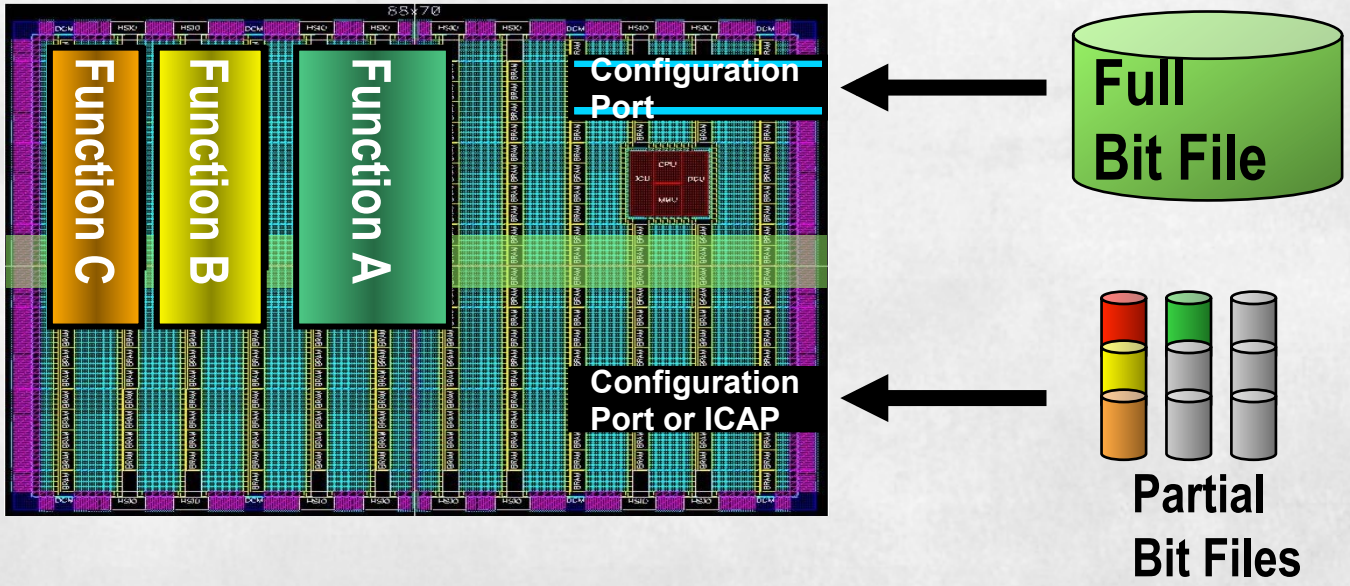
- SW components
  - GnuRadio with HW acceleration capabilities – RFNoC
  - Reconfiguration Capabilities
- SW – HW interface
  - shared memory
  - separate ***control*** and ***data plane*** interfaces



Hardware accelerated SDR platform on top of Hybrid FPGA (3)

- Real time re-configurability
  - *Partial reconfiguration via PCAP*





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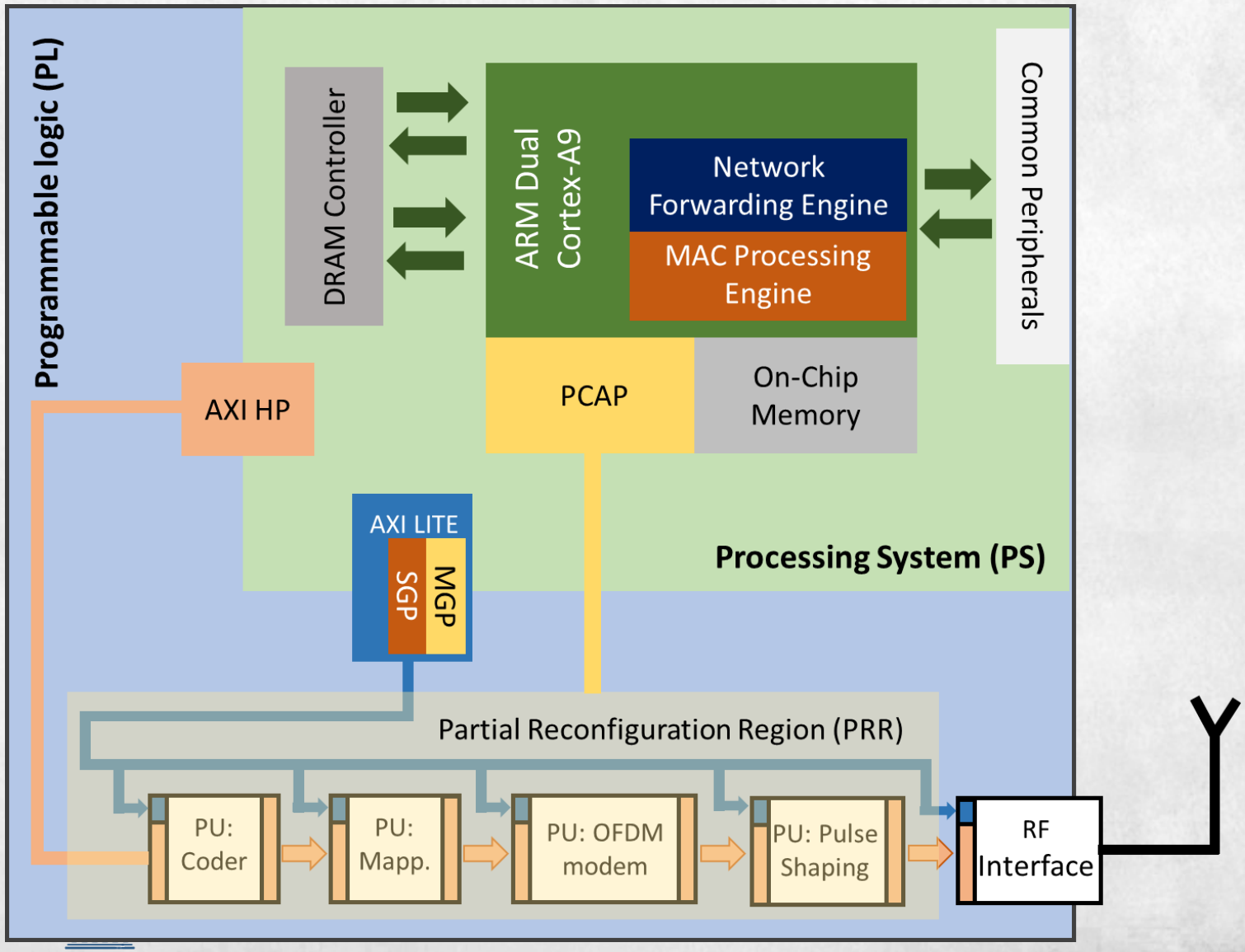
Hardware accelerated SDR platform on top of Hybrid FPGA (4)



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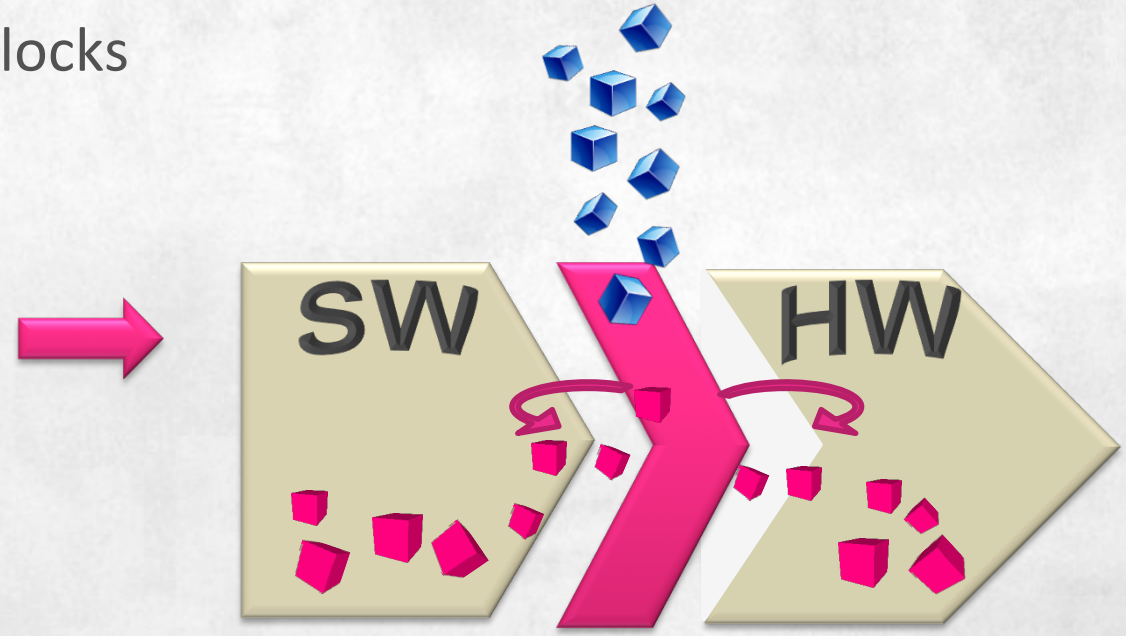
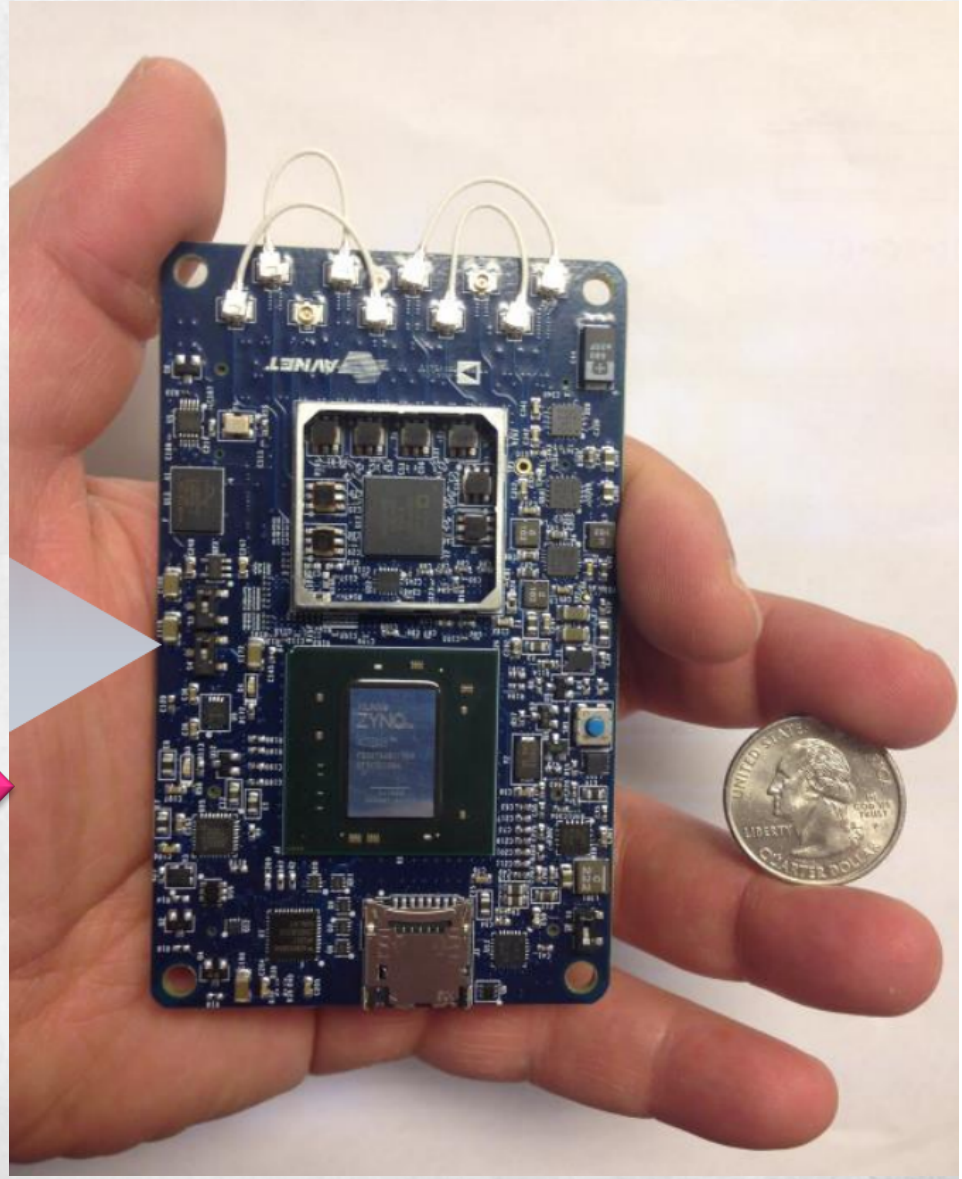
Hardware accelerated SDR platform on top of Hybrid FPGA (5)

- **This concept enables**
  - ***Offload*** of SW Radio blocks to FPGA
  - ***Frees up processor*** to perform other tasks



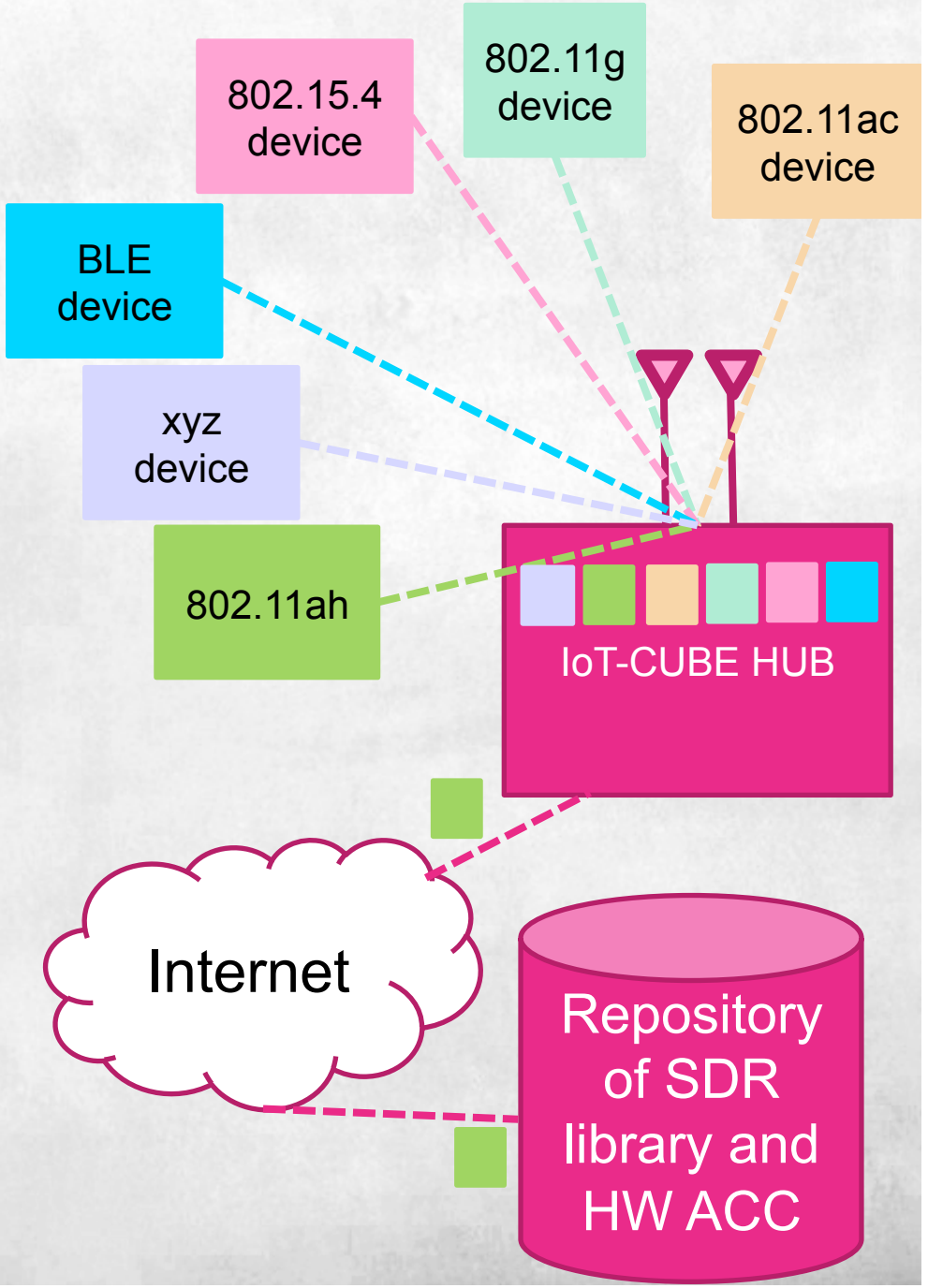
Hardware accelerated SDR platform on top of Hybrid FPGA (6)

- **This concept enables**
  - ***Offload*** of SW Radio blocks to FPGA
  - ***Frees processor*** to perform other tasks
  - Whole SDR system should fit on ***one board***



Example Scenario

- **Different applications – different wireless standards**
  - Our platform should support various ***existing*** and ***future*** emerging wireless technologies at same time
    → ***IoT HUB***
  - Download SDR packages from cloud → ***Air Interface as a Service***



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Questions?